means for adjusting the frequency at which the local clock oscillates, when there is at least one of said differences, so that said at least one of said differences approaches zero;

wherein the means for adjusting the frequency at which the local clock oscillates includes:

hardware for adjusting the local clock frequency until a threshold condition occurs; and

a processor having a software program for adjusting the local clock frequency after the threshold condition occurs.

13. (Four Times Amended) A system for synchronizing the frequency of a local clock of a digital data decoder with the frequency of a program clock, comprising:

means for determining if there is any difference between the local and program clock frequencies; and

means for adjusting the frequency at which the local clock oscillates, when there is a difference between the local clock and the program clock frequencies, so that said difference approaches zero, wherein the means for adjusting includes

i) hardware on the decoder for adjusting the local clock frequency until a threshold condition occurs, and

ii) a processor on the decoder and having a software program for adjusting the local clock frequency after the threshold condition occurs.

REMARKS

In the Office Action, the Examiner allowed Claim 1, objected to Claim 2, and rejected Claims 3-5, 7-10 and 13-15 under 35 U.S.C. §112 as being indefinite.

Claims 2, 3, 7 and 13 are herein being amended to overcome the objection to Claim 2 and the rejection of Claims 3-5, 7-10 and 13-15.

More specifically, Claim 2 is being amended, as the Examiner suggested, to change "said difference" in lines 11 and 12 to "said absolute difference". This overcomes the objection to Claim 2, and the Examiner is thus asked to reconsider and to withdraw the objection to this claim.

Claim 3 is being amended to delete unnecessary language, and to change "said difference" to said absolute difference" in lines 15 and 16. Applicant believes that this overcomes the Examiner's objection to Claim 3 and Claims 4 and 5, which are dependent from Claim 3.

Claim 7 is being amended to rephrase the description of the determining means, and in particular, to refer to "at least one of" two defined differences. Also, the description of the adjusting means is being rephrased to indicate that the frequency of the local clock is adjusted so that said "at least one of" those differences approaches zero. It is submitted that these changes to Claim 7 fully address the Examiner's objection to this Claim and to Claims 8-10, which are dependent from Claim 7.

Claim 13 is being amended to delete the reference to the local clock value and the program clock value. It is noted that Claim 13 includes limitations analogous to those set forth in allowable claim 1, and remains allowable over the prior art. The changes made herein to Claim 13, it is believed, overcome the rejection of Claim 13-15 under 35 U.S.C. §112.

Applicant's Attorneys have carefully reviewed all of the pending claims 1-5, 7-10 and 13-15, and the claims, as amended herein, are clear and definite and fully comply with the requirements of 35 U.S.C. §112. The Examiner is, accordingly, respectfully requested to

reconsider and to withdraw the objection to Claim 2 and the rejections of Claims 3-5, 7-10 and 13-15 under 35 U.S.C. §112, and to allow Claims 1-5, 7-10 and 13-15.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**Version with markings to show changes made.**"

Every effort has been made to place this case in condition for allowance, a notice of which is requested. If the Examiner believes that a telephone conference with Applicant's Attorneys would be advantageous to the disposition of this case, the Examiner is asked to telephone the undersigned.

Respectfully Submitted,

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Serial No: 09/052,673 **Docket:** END919980042US1(11232)

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Claims 2, 3, 7 and 13 have been amended as follows:

--2. (Twice Amended) A method according to Claim 1, wherein the local clock oscillates at the local clock frequency, the method further comprising the steps of:

maintaining a local clock value based on the oscillations of the local clock;

receiving clock time stamps at the decoder which specify the program clock signals and the frequency of the program clock;

maintaining a program clock value based on the program clock signals received at the decoder;

determining if there is an absolute difference between the local clock value and the program clock value;

if there is an absolute difference between the local clock value and the program clock value, then adjusting the frequency at which the local clock oscillates so that said absolute difference approaches zero.

3. (Four Times Amended) A method of synchronizing the frequency of a local clock of a digital data decoder with the frequency of a program clock, wherein the local clock oscillates at a local clock frequency, the method comprising the steps of:

determining the difference between the local and program clock frequencies, then adjusting the frequency at which the local clock oscillates so that said difference approaches zero;

maintaining a local clock value based on the oscillations of the local clock;

receiving clock time stamps at the decoder which specify program clock signals and the program clock frequency;

maintaining a program clock value based on the program clock signals received at the decoder;

[determining if there is any difference between the local clock frequency and the program clock frequency;]

determining if there is an absolute difference between the local clock value and the program clock value;

if there is [either a difference between the local clock frequency and the program clock frequency or] an absolute difference between the local clock value and the program clock value, then adjusting the frequency at which the local clock oscillates so that said absolute difference approaches zero;

wherein the decoder includes hardware for adjusting the local clock frequency and a processor having a software program for adjusting the local clock frequency, and wherein the step of adjusting the frequency of the local clock includes the steps of:

using the hardware to adjust the local clock frequency until a threshold condition occurs; and

after the threshold condition occurs, using the processor to adjust the local clock frequency.

7. (Twice Amended) A system for adjusting a local clock on a digital data decoder, wherein the clock oscillates at a local clock frequency, the system comprising:

7. (Twice Amended) A system for adjusting a local clock on a digital data decoder, wherein the clock oscillates at a local clock frequency, the system comprising:

means for maintaining a local clock value based on the oscillations of the local clock;

means for receiving clock signals transmitted to the decoder at a program clock frequency;

means for maintaining a program clock value based on the clock signals transmitted to the decoder;

means for determining if there is at least one of (i) a [any] difference between the local clock and the program clock frequencies, and (ii) an absolute difference between the local clock value and the program clock value; and

[means for determining if there is an absolute difference between the local clock value and the program clock value; and]

means for adjusting the frequency at which the local clock oscillates, when there is [a difference between the local clock and the program clock frequencies or an absolute difference between the local clock value and the program clock value] at lease of one of said differences, so that said [difference] at least one of said differences approaches zero;

wherein the means for adjusting the frequency at which the local clock oscillates includes:

hardware for adjusting the local clock frequency until a threshold condition occurs; and

a processor having a software program for adjusting the local clock frequency after the threshold condition occurs.

13. (Times Amended) A system for synchronizing the frequency of a local clock of a digital data decoder with the frequency of a program clock, comprising:

means for determining if there is any difference between the local and program clock frequencies; and

[means for determining if there is an absolute difference between the local clock value and the program clock value; and]

means for adjusting the frequency at which the local clock oscillates, when there is a difference between the local clock and the program clock frequencies, [or an absolute difference between the local clock value and the program clock value,] so that said difference approaches zero, wherein the means for adjusting includes

i) hardware on the decoder for adjusting the local clock frequency until a threshold condition occurs, and

ii) a processor on the decoder and having a software program for adjusting the local clock frequency after the threshold condition occurs.